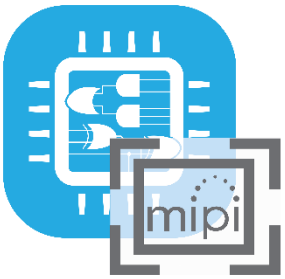
PRESS RELEASE – MIPI CSI-2

For immediate release – September 2019

New MIPI CSI-2 Receiver IP Core from Sensor to Image



MIPI CSI-2 is one of the most widely used camera sensor interfaces. Many applications require the connection to an FPGA for advanced image pre-processing and further transfer to a host system. Sensor to Image's MIPI CSI-2 Receiver IP core provides a solution for decoding video streams from CSI-2 sensors in a Xilinx FPGA. In order to shorten the development time, the IP core is delivered with a fully working reference design including Sensor to Image's MVDK and an IMX274 MIPI FMC module.

MIPI CSI-2 Receiver IP Core

IP Core for MIPI CSI-2 Imagers

AT A GLANCE

- MIPI CSI-2 receiver and decoding block
- Configurable number of MIPI Lanes
- Using Xilinx D-PHY IP
- Delivered with a reference design for fast development

More info: https://www.euresys.com/en/Products/IP-Cores/Sensor-IP-Cores/MIPI-CSI-2-Receiver-IP-Core

More info about Euresys and Sensor to Image please visit: https://www.euresys.com/Homepage

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